IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Zhong Dong, Chuck Jang, Ching-Hwa Chen		
Assignee:	Mosel Vitelic, Inc.		
Title:	Floating Gate Nitridation		
Serial No.:	10/769,025	Filing Date:	January 30, 2004
Examiner:	Pizarro-Crespo, Marcos D	Group Art Unit:	2814
Docket No.:	M-12327-3C US	Confirm:	7632

San Jose, California

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

DECLARATION OF JASON B. TAYLOR TRAVERSING GROUNDS OF REJECTION

PURSUANT TO 37 C.F.R. §1.132

Dear Sir:

I, Jason B. Taylor, declare as follows:

1. My current residence address is 5022 Rigatti Circle, Pleasanton, CA 94566.

OCCUPATIONAL AND EDUCATIONAL CREDENTIALS

2. I am currently an employee of the assignee in interest of the above-identified patent application, said assignee being Mosel Vitelic Corp. ("Mosel") with offices in Santa Clara California. My work for Mosel spans the following time periods: May 2004 to present (Job Title: Staff Engineer).

3. Immediately before starting with

4. I have been working in the semiconductor industry for at least 8 years . I began working at Micrel Semiconductor in 1997. Over the years I have had extensive

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

experience with ion implant and surface treatment technologies. This experience includes working with various ion implanters and plasma deposition tools.

5. I am familiar with the invention disclosed in the above-referenced U.S. Application Serial No. 10/769,025 that names Zhong Dong and others as inventors.

6. I have the following formal college degrees: BS Chemical Engineering, San Jose State University (1994), MS Chemical Engineering, San Jose State University (1997), MS Engineering, Microelectronic Materials and Devices, San Jose State University (2005).

DOCUMENTS REVIEWED

7. In preparing for making this Declaration, I reviewed the following documents, the first of which was cited in the prosecution of application Serial No. 10/769,025:

(a) **Lin** U.S. Patent No. 6,127,227;

(b) **Misium** U.S. Patent No. 6,261,973;

(c) Misium U.S. Patent No. 6,140,024 (aka **George**); and

(d) Zheng U.S. Patent No. 6,653,199.

8. I have reviewed the specification and drawings of the present U.S. patent application Serial No. 10/769,025 both in its original form and amended form (with latest claims).

9. I have further reviewed the final Office Action dated 5/17/2005 (hereafter also "May '05 OA") in the subject U.S. patent application Serial No. 10/769,025.

10. I have yet further reviewed Claims 1-25 as presented in Applicant's Response of April 2005 and the attorney arguments presented in that 4/2005 Response.

11. Additionally, I make reference herein to the following textbooks or authoritative publications, which I submit are relevant to understanding how a person

acPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

of ordinary skill would have viewed the art at the relevant time (before the effective date of parent application 10/071,689 filed Feb. 8, 2002:

(11a) "ULSI Technology", Chang and Sze, 1996 McGraw-Hill, ISBN 0-07-114105-7 (including Figure 3 on page 476 of this textbook **(Copy appended hereto)** where this figure buttresses my finding that Lin's Fig. 2B is indicative of an energetic ion implantation below the surface).

OFFICE ACTION REVIEWED

12. As I am given to understand, in the Office Action of 5/17/2005 (May '05 OA) the examining official (hereafter "Examiner") at the U.S. Patent and Trademark Office (hereafter "PTO") asserted either expressly or by implication that a person of ordinary skill in the art at a time prior to February 2002 (the effective filing date of the Dong patent application) would have been motivated to combine what such a person read in the Lin '227 reference with what such a person read in the Misium '973 document and in the Misium '024 (aka George) reference and would have then been motivated to produce, without aid of hindsight, the subject matter defined by Claim 1 of the subject U.S. patent application, Serial No. 10/769,025 (Dong et al). The PTO made further assertions about others of the claims.

13. Referring to claim 1 and specifically to page 3, last full paragraph of the May 2005 OA, the PTO appears to view the Lin '227 reference as teaching at col. 4 lines 39-46 to use "a nitrogen treatment **or** ion implantation" (emphasis added) where the emphasized "or" is taken in the disjunctive sense, meaning the PTO believes the ordinary artisan would have seen col. 4 lines 39-46 as providing two options: one where ion implantation is used and a second where another "treatment" such as surface nitridation is an alternate possibility.

14. Since these relied-upon paragraphs in Lin '227, namely, col. 4, lines 39-etc. are vital to the construction of the rejection, they are reproduced immediately below with emphasis added:

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

> As a main feature and **key aspect** of this [Lin's] invention, the polysilicon layer is then subjected to nitrogen treatment **as shown in FIG. 2b.** The nitrogen treatment is accomplished at a pressure between about 400 to 600 millitorr (mT). In a second embodiment, the first polysilicon layer is subjected to **ion implantation** at a dosage level between about 1.times.10.sup.12 to 5.times.10.sup.14 atoms/cm.sup.2 at **an** energy between about 5 to 30 KeV. It will be appreciated that the **presence** of nitrogen, **shown as phantom dots** (125) in FIG. 2b, in the upper layers of polysilicon (120) will suppress the oxidation rate of polysilicon, thereby providing an enhanced **control** of the thickness of the bottom oxide of the ONO composite that is to be formed next over the first polysilicon layer. In essence, the thickness of the bottom oxide of the ONO layer to be formed **is controlled** by still another very thin layer formed through the combination of **the nitrogen introduced** into the first polysilicon layer with silicon and the **oxidizing oxygen** of the next step. This additional thin layer thus forms an augmented ONO layer.
>
> Thus, the bottom oxide layer (143) in FIG. 2c, of the to be augmented ONO layer, is next formed by first subjecting the **nitrogen rich** first polysilicon layer to oxidation, preferably at a temperature between **about 700 to 1050.degree.C**. However, **at the same** that the bottom oxide layer is **grown**, still another, but an unusually thin augmented layer (130) is formed having a composition of **nitrogen**, oxygen and silicon (N--O--Si). **The thickness of the N--O--Si layer is only between about 5 to 10 .ANG., while the overlying bottom oxide assumes a thickness of between about 40 and 120 .ANG.**. It will be apparent to those skilled in the art that the unusual thinness of the augmented layer (130) **along with** the thin and uniform thickness of the bottom oxide layer (143) of the augmented ONO then makes it possible to attain **the precise coupling ratio** that is **required** for the accurate performance of the memory cell. Also, while nitrogen in the first polysilicon slows down the polysilicon oxide growth for thin augmented ONO formation, it suppresses the gradual gate oxidation (GGO) effect in the floating gate. This in turn is found to increase gate coupling ratio as well as improving charge retention of the cell. [emphasis added]

15. At page 10, last full paragraph of the May 2005 OA, the PTO makes clear its final position that "applicants failed to notice that said technique [*the subsurface ion implant one*] **is but one of the two processes** disclosed by Lin. Lin is not restricted to said implantation technique." [Emphasis and bracketed text added.] As I understand it, a critical underpinning of the PTO rejection is the PTO's belief that Lin discloses two processes. From a technical stand point, this belief is wrong; as I will demonstrate in detail below.

16. I do not hold myself out as an expert in the field of patent law and thus I will not pass judgment on the ultimate legal conclusion of "obviousness". That is for the

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

attorneys to argue. However, I do have personal experience and expertise as an artisan in the field of semiconductor fabrication, and in particular in the areas of ion implantation, surface treatment and the understandings of those skilled in the art, especially just prior to February 2002 (the critical date for the present Dong application).

17. Based on my expertise, I find the PTO position to be wholly untenable. It is outside of reason and logic to propose that the ordinary artisan (who is, as I am given to understand, a hypothetical creature of law, existing only in the past) would have read Lin '227 as teaching "that ... [the subsurface ion implant one] **is but one of the two processes** ".

18. In my expert opinion, subsurface ion implantation *is the only process* that Lin '227 taught to the ordinary artisan at the relevant time. Ion implantation is the "main feature and key aspect of [Lin's] invention" --see the opening text of the above reproduction (Lin col. 4, line 39).

19. My opinion is based on the following parsing of the reproduced text. First, it should be observed that the mention in Lin of: "In a second embodiment, ..." (Lin col. 4, line 43) is a clear typographic error since there is no "first embodiment" described anywhere in Lin '227. A person of ordinary skill would have clearly ignored this obvious typographic error as being of no consequence.

20. Second, Lin refers to Fig. 2B when he states at col. 4, line 39-41: "the polysilicon layer is then subjected to nitrogen treatment **as shown in FIG. 2b.**" [Emphasis added.] Fig. 2B shows charged nitrogen particles ("N+") being projected downwardly into the polysilicon layer 125. The person of ordinary skill would have viewed this schematic diagram as clearly teaching the use of ion (charged particle) acceleration and implantation. (See also the appended copy of Figure 3 of page 476 of "ULSI Technology", by Chang and Sze, as cited above, which Fig. 3 demonstrates an example of this type of ion implant diagram.) There is no suggestion in Fig. 2B of anything other than an ion implant step. There are no enabling details given regarding an alternate treatment method. Moreover, Lin expressly states that the nitrogen ions should be implanted at a singular energy when he states, "[T]he first polysilicon layer

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

is subjected to ion implantation ... at **an** energy between about 5 to 30 KeV." (Col. 4, line 45.) The article "an" denotes that a single magnitude of implant energy is to be selected. It is to be selected from the range of "about 5 to 30 KeV." That selection will determine how deep under the surface the implanted ions will come to lie. That depth will in turn define the thickness of "the overlying bottom oxide ... between about 40 and 120 .ANG." (col. 4, line 68). The thickness is critical to the operability of Lin's invention. As explained at col. 5, line 5, it is the precise control over the thickness of the augmented layer and the precise control over the thickness of the overlying oxide that allows one to control the capacitive coupling ratio in the memory cell.

21. Another reason why the PTO's position is untenable is because Lin's Fig. 2B cannot be viewed in isolation. It is clearly the direct precursor to the structure shown in Fig. 2C. It is undisputable that in Fig. 2C, a darkened and thick line 130 is shown below the surface of oxide layer 143. One skilled in the art will readily understand that this thick line 130 represents the "augmented region" as Lin calls it, and that its internal contents are composed of a silicon oxynitride composition (or " N--O--Si" as Lin refers to it). There is no silicon oxynitride above line 130. Instead there is only silicon oxide in region 143. (Lin refers to region 143 as "the bottom oxide layer (143)".) The silicon atoms found in region 143 could have come from only one place, namely, that part of Fig. 2B above dashed line 125, which is part of the deposited polysilicon layer 120. Since there is no nitrogen in the "silicon oxide" composition of region 143, this is proof positive that Lin clearly teaches to not have nitrogen above dashed line 125.

22. By contrast, in the May 2005 OA, the PTO asserts at page 10: "Lin lacks any teaching describing the region above line 25 [sic] as being free of nitrogen." This fact finding by the PTO is clearly erroneous as I have demonstrated immediately above. It appears to me that the PTO is twisting the unambiguous guidance of Lin like a nose of wax to make it mean something completely different from how a person of ordinary skill would have seen it.

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

23. Going back to the meaning of the dashed line 125 in Lin Fig. 2B, Lin writes at col. 4, lines 46-47: "It will be appreciated that the presence of nitrogen, shown as phantom dots (125) in FIG. 2b, ...". In my expert opinion, the reasonable person of

ordinary skill could only have interpreted this at the relevant time to mean that the implanted nitrogen atoms are restricted to lying only at the depth represented by dashed line 125. It is not a boundary. It is an implant depth. It is where the nitrogen lies buried. That's what the word "presence" implies. See again the appended copy of Figure 3 of page 476 of "ULSI Technology" cited in 11(a) of this document for an example of a figure also used in this manner.

24. By contrast, in the May 2005 OA, the PTO argues at page 10: "The dashed line 125 is used to indicate the upper layers of the polysilicon layer 120 wherein the nitrogen is present (...) As seen in Fig. 2A the upper layers of the polysilicon layer include its surface." In my opinion, this line of argument is an illusion and a coy play with words. Polysilicon layer 120 is composed only of polysilicon. There are no "layers" of polysilicon prior to the implant of the nitrogen ions. After the nitrogen ions are implanted, that one very thin layer of nitrogen atoms, which layer is represented by dashed line 125 divides the original polysilicon deposition 120 into a lower layer of just polysilicon where the lower layer lies below the layer 125 of implanted nitrogen atoms and into an upper layer of just polysilicon, located above the implanted nitrogen atoms. Thus by using the term, layers, the PTO is inherently admitting that the material above line 125 does not contain nitrogen. That is exactly how a person of ordinary skill in the art would have understood Lin. There is no nitrogen above line 125. Dashed line 125 is the implanted nitrogen.

25. After implant, and upon heating to "a temperature between about 700 to 1050.degree.C." (Lin col. 4, line 61) in an oxidizing atmosphere, the nitrogen rich line 125 is converted into oxynitride layer 130 (Fig. 2B) and the nitrogen free layer above line 125 is converted to silicon oxide. The lower polysilicon layer below line 125 is not converted to silicon oxide because, as Lin himself explains, "[the] nitrogen [layer 125] in the first polysilicon [120] slows down the polysilicon oxide growth for thin augmented ONO formation" (col. 5 ,lines 6-7, bracketed text added for readability).

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

26. Thus to summarize my findings thus far: there is no reasonable basis for concluding that a person of ordinary art would have read Lin at the relevant time as teaching or suggesting alternate nitrogen treatments. There is only one nitrogen treatment and it is an energetic implantation of nitrogen atoms into a singular layer

125 (Fig. 2A) lying a given depth below the surface of polysilcon 120. There are, for all intents and purposes, no nitrogen atoms above line 125. That is why the polysilicon becomes silicon oxide rather than an oxynitride during the high temperature oxidation step. Only the thickness of line 130 represents an oxynitride and it is clearly spaced below the top surface of polysilicon 120.

27. As I understand it, the PTO next proposes that the teachings of Lin are to be combined with those of Misium '973 and Misium '024 (aka George). The motivation used for justifying this proposed combining of unrelated technical disclosures is that "Misium ['973] clearly teaches RPN is an improved low-temperature ion-implantation step that can be used for creating Lin's nitrided layer." (May 2005 OA, page 11, emphasis added.)

28. From my review of Misium '973 I see no such teaching and a reasonable person of ordinary skill would not have seen it either. First, Misium '973 never talks about using RPN to introduce nitrogen atoms below a substrate surface. In RPN, the nitrogen atoms are introduced only "on" the surface ---see Misium '973 at col. 2, line 25. Fig. 3C of Misium '973 clearly shows that the RPN provided nitrogen "creates a nitrided layer 22" (col. 4, line 26) only on top of the surface and not at a depth below the surface. Lin requires that nitrogen atoms be energetically accelerated to penetrate and come to a stop below the surface. Misium '973 does not anywhere teach that RPN "can be" used to create such a buried layer of nitrogen atoms and no person of skill in the art would reasonably read Misium '973 as teaching that. The PTO's assertion that RPN "can be" used to form the buried nitrogen layer of Lin is not only unfounded, it is factually wrong. In addition, Misium '973 clearly shows the nitrogen treatment being performed on top of an oxide layer, not a silicon or polysilicon layer. The purpose of Misium's layer is fundamentally different from Lin's, and no reasonable connection between the two would be apparent to a person of ordinary skill.

29. With regard to Zheng (US 6,653,199) which was applied against claim 11 due to its mention of DPN, basically the same arguments apply as with regards to RPN. Both are surface treatments and do not of themselves produced a buried oxynitride layer in accordance with the teachings of Lin. I do not see anything in the record other than use of 20/20 hindsight that could have motivated an ordinary artisan at the

acPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

relevant time to consider the surface treatments of Misium '973 (RPN on silicon surface), Misium '024 --aka George '024-- (RPN on silicon oxide surface) and Zheng '199 (DPN) to be in the same camp with the energetic implant and thermal anneal teachings of Lin. An advantage of RPN and DPN is that they can be practiced at low temperature. It goes against common sense in the art to use a low temperature surface nitridation process like RPN or DPN and then follow it up with a high temperature anneal. The thermal anneal takes away the thermal budget gains attained with the RPN or DPN.

30. As stated above, I do not hold myself out as being an expert in patent law. However, I am given to understand that when a "rejection" is based on factually incorrect findings, then that rejection must collapse just as surely as a building constructed on mythical foundations must collapse. The above should therefore be sufficient to collapse all rejections against claims 1-25.

31. I have reviewed the arguments made by the attorney in the April 2005 response. In so far as the nonlegal technical arguments made, they are all sound. My above and more detailed analysis above bears out what the attorney was arguing regarding proper interpretation of the teachings of Lin, Misium '973 (RPN on silicon surface), Misium '024 --aka George '024-- (RPN on silicon oxide surface) and Zheng '199 (DPN). As to the legal arguments about "criticality," I will not render an opinion about that.

32. As part of the rebuttal against Applicants arguments, the PTO states in the May 2005 OA, at page 11, around lines 3-4: "Regarding the buried layer, see comments sated above in paragraph 25 ... repeated here." I for one, do not see how arguing that Lin has an undefined, second treatment (which he does not), addresses the issue of forming a buried nitrogen layer at a precise distance below the surface of the polysilicon layer. That is one of the key points that Lin is making to those skilled in the art. By precisely setting the implant energy "at" a particular level, Lin forms a buried layer of nitrogen atoms and a layer of precise thickness above it that has silicon, but no nitrogen atoms. Then during thermal oxidation, the nitrogen-free poly above the buried nitrogen atoms is converted into silicon oxide. When the oxidation front hits the buried nitrogen layer, advancement of the oxidation front is suppressed,

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

as Lin clearly states (col. 4, line 48) and the oxynitride layer 130 is formed. No oxidation takes place below the nitrogen-rich layer 125. It is by this means that Lin defines the thickness of the silicon oxide formed above layer 130. It is by this means that Lin defines the critical capacitive coupling ratio of his memory cell.

33. As part of the rebuttal against Applicants arguments, the PTO states in the May 2005 OA, at page 12, around lines 9-10: "Lin shows the presence of nitrogen in the nitrided surface but fails to specify the nitrogen concentration." That is false on both counts. Lin does specify the concentration. It is ZERO. There is no nitrogen above the buried layer 125. Lin does not have a nitrided "surface". He has an energetically nitrided, buried layer 125, which upon thermal oxidation becomes the buried oxynitride layer 130. I do not see how a person of ordinary skill in the art it could see it otherwise.

34. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 11th day of July in the year 2005

at San Jose, Santa Clara County, California

(city/county and state)

(Signature) Jason B. Taylor

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Appendix (Copy of pending claims)

CLAIMS LISTING (all of pending claims 1-3, 10-25)

Claim 1 (*Previously Presented*): A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming a conductive first layer containing primarily silicon, the first layer being to provide one or more floating gates for the nonvolatile memory;

(b) nitriding a silicon-containing surface of the first layer with a low temperature, low energy, surface nitriding process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said silicon-containing surface of the first layer at relatively low temperature and relatively low energy;

(c) subjecting the nitrided surface to a thermally oxidizing atmosphere so as to thereby form a thermally-grown silicon oxide at the nitrided surface, the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms defining at least part of a first dielectric of the nonvolatile memory; and

(d) forming a conductive second layer separated by the first dielectric from conductive material of the first layer, the conductive second layer providing one or more control gates for the nonvolatile memory.

Claim 2 (*Previously Presented*): The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises performing oxidation at a temperature in the range 800°C-1050°C in an oxygen or oxygen/hydrogen atmosphere to thereby form the silicon oxide by thermal oxidation.

Claim 3 (*Original*): The method of Claim 1 wherein the surface of the first layer is a polysilicon surface.

acPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claims 4-9 (*Canceled*)

Claim 10 (*Previously Presented*): The method of Claim 1 wherein the nitriding step includes using a Remote Plasma Nitridation (RPN) process.

Claim 11 (*Previously Presented*): The method of Claim 1 wherein the nitriding step includes using a Decoupled Plasma Nitridation (DPN) process.

Claim 12 (*Previously Presented*): The method of Claim 1 wherein the nitriding step provides a concentration of nitrogen atoms of 1-20 atomic percent in the nitrided surface.

Claim 13 (*Previously Presented*): The method of Claim 12 wherein the nitriding step incorporates said nitrogen atoms to a depth of no more than 3 nm in said surface of the first layer.

Claim 14 (*Previously Presented*): The method of Claim 1 wherein said first layer is disposed over a tunneling dielectric.

Claim 15 (*Previously Presented*): The method of Claim 14 and further comprising: thermally growing the tunneling dielectric.

Claim 16 (*Previously Presented*): The method of Claim 1 and further comprising: depositing a silicon nitride layer on said combination of the thermally-grown silicon oxide and incorporated nitrogen atoms to thereby define a further part of the first dielectric of the nonvolatile memory.

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claim 17 (*Previously Presented*): The method of Claim 16 and further comprising:

depositing a silicon oxide layer on said deposited silicon nitride layer to thereby define a yet further part of the first dielectric of the nonvolatile memory.

Claim 18 (*Previously Presented*): A method of manufacturing a nonvolatile memory cell within a monolithically integrated circuit, the method comprising:

(a) forming a tunneling dielectric layer on a semiconductive substrate;

(b) forming a floating gate layer on said tunneling dielectric layer, the floating gate layer having a top surface composed primarily of conductive silicon;

(c) surface nitridating said top surface of the floating gate layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said top surface of the floating gate layer at relatively low temperature and relatively low energy; and

(d) subjecting the nitrided top surface to a thermally oxidizing atmosphere so as to thereby form a combination of thermally-grown silicon oxide and surface incorporated and thermally treated nitrogen atoms at the nitrided and thermally oxidized top surface of the floating gate layer.

Claim 19 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further comprising:

(e) depositing a silicon nitride layer directly on the nitrided and thermally oxidized top surface of the floating gate layer.

Claim 20 (*Previously Presented*): The memory cell manufacturing method of Claim 19 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claim 21 (*Previously Presented*): The memory cell manufacturing method of Claim 19 and further comprising:

(f) depositing a silicon oxide layer directly on the silicon nitride layer.

Claim 22 (*Previously Presented*): The memory cell manufacturing method of Claim 21 and further comprising:

(g) surface nitridating said deposited silicon oxide layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said deposited silicon oxide layer at relatively low temperature and relatively low energy.

Claim 23 (*Previously Presented*): The memory cell manufacturing method of Claim 22 and further comprising:

(h) forming a conductive gate layer on said surface nitridated and deposited silicon oxide layer.

Claim 24 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

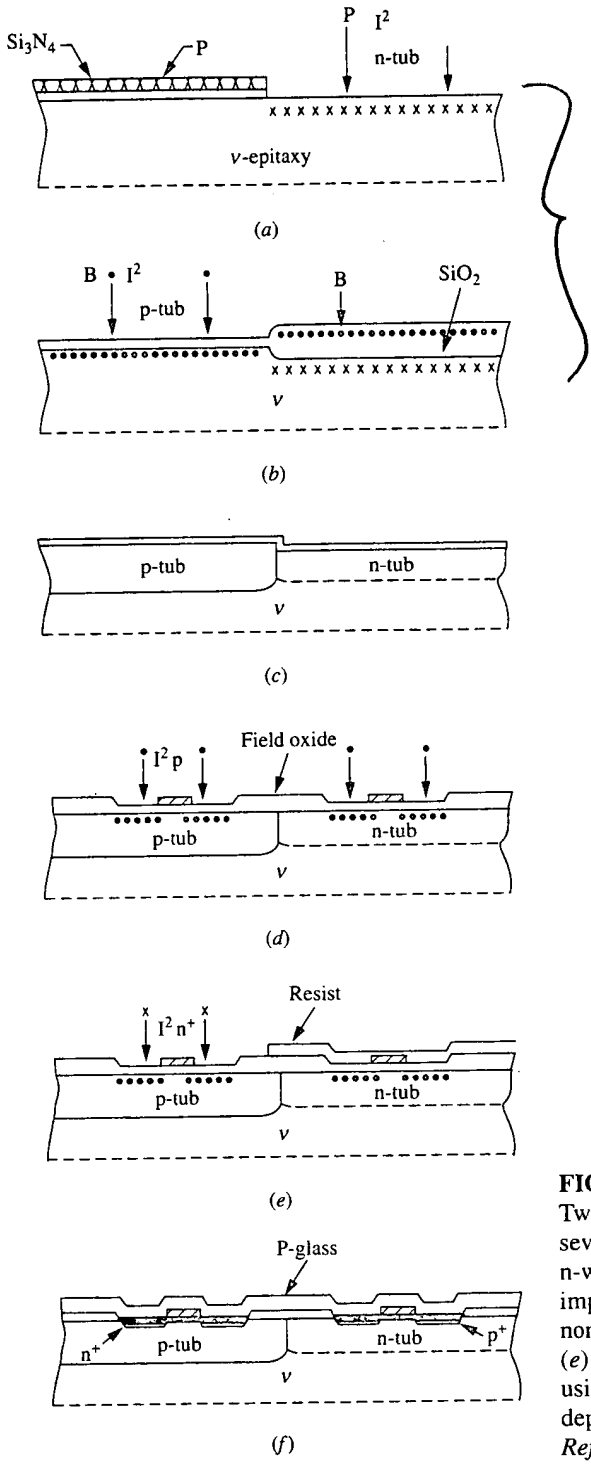
Claim 25 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further wherein:

said surface nitridating step incorporates nitrogen atoms into the said top surface of the floating gate layer to a depth of less than 3nm.

***

acPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

EXHIBIT "A"



Typical diagram showing implanted species (compare to FIG 2B IN LIN PATENT)..

FIGURE 3
Twin-well CMOS structure at several stages of the process: (*a*) n-well ion implant (I^2); (*b*) p-well implant; (*c*) twin-well drive-in; (*d*) nonselective p^+ source/drain implant; (*e*) selective n^+ source/drain implant using photoresist mask; (*f*) P-glass deposition. (*After Parrillo et al., Ref. 4.* ©1980 IEEE.)

McGraw-Hill

A Division of The McGraw-Hill Companies

ULSI TECHNOLOGY
International Editions 1996

Acknowledgements begin on page 724 and appear on this page by reference.

3 4 5 6 7 8 9 0 CWP UPE 9 8 7

ISBN 0-07-063062-3

This book was set in Times Roman by Publication Services, Inc.
The editors were Lynn Cox and John M. Morriss;
the production supervisor was Denise L. Puryear.
The cover was designed by Farenga Design Group.
Project supervision was done by Publication Services, Inc.

Cover photo: Electron micrograph of contact holes filled with CVD tungsten plugs (see Chapter 8). The diameter is 0.25 micron. *Courtesy of the National Nano Device Laboratories. National Science Council, R.O.C.*

Library of Congress Catalog Card Number: 95-81366

When ordering this title, use ISBN 0-07-114105-7

Printed in Singapore

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☑ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.